SGS-THOMSON MICROELECTRONICS

ST14E32F
ST15E32F

SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I2C BUS 32K (4K x 8)EEPROM

- COMPATIBLE WITH I2C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES, OVER THE FULL SUPPLY VOLTAGE RANGE
- 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V FOR THE ST14E32F
  - 2.7V to 5.5V FOR THE ST15E32F
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (UP TO 32 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

Figure 1 Delivery forms

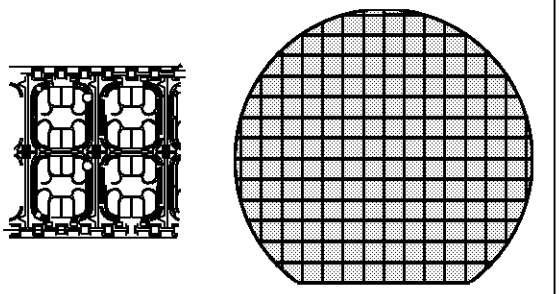
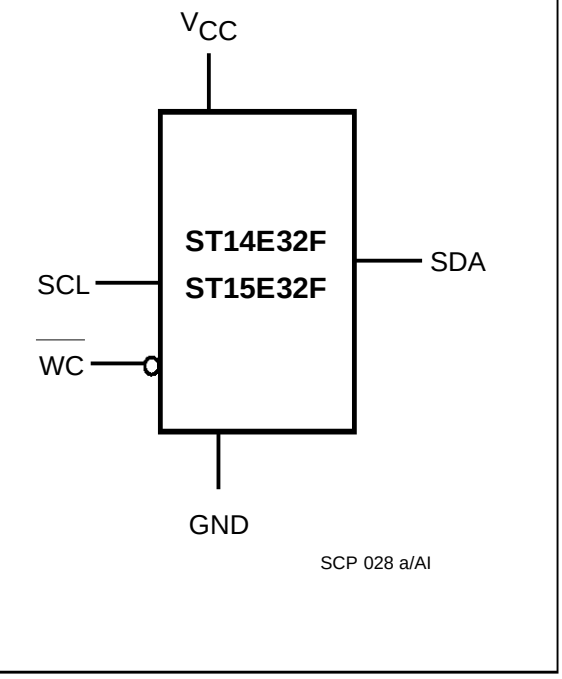


Figure 2 Pin Connection



DESCRIPTION

The ST14/15E32F are 32K bit electrically erasable programmable memory products (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST15E32F circuit operates with a power supply value as low as 2.7V. Both wafer and micromodule forms are available.

Table 1 Signal Names

SDA	Serial Data Address Input Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
GND	Ground

The ST14/15E32F are compatible with the I2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock.

The ST14/15E32F carry a built-in 4 bit, unique device identification code (1010) corresponding to the I2C bus definition.The ST14/15E32F behave as a slave device in the I2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master.

The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/ write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Figure 3 Contact Connections

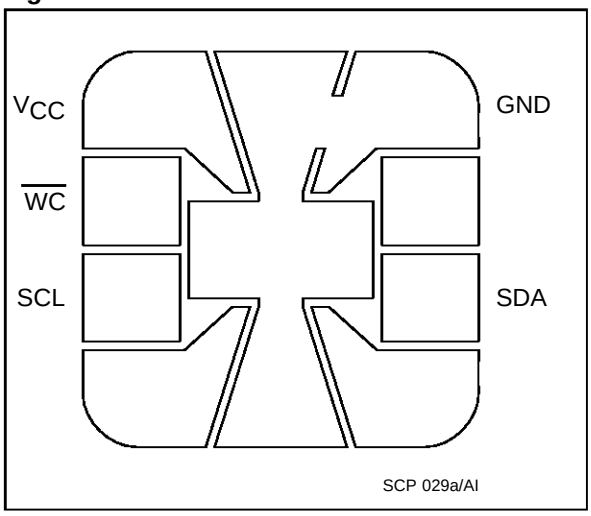


Figure 4 Die Floor Plan

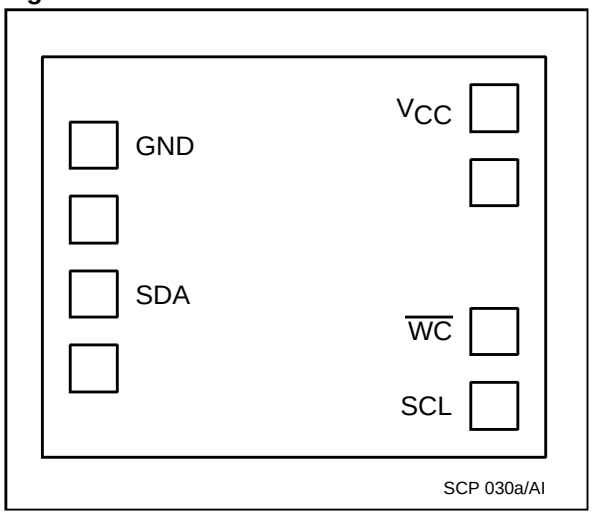


Table 2 Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature Wafer form Module form	-65 to 150 -40 to 120	°C
V_{IO}	Input or Output range	-0.3 to 6.5	V
V_{CC}	Supply Voltage	-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	4000	V
	Electrostatic Discharge Voltage (Machine model) (3)	500	V

Notes : 1) Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2) MIL-STD-883C, 3015.7 (100pF, 1500 Ohm).

3) EIAJ IC-121 (Condition C) (200pF, 0 Ohm)

Power On Reset : VCC lock out write protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command.

In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 3 Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$R\overline{W}$

Note : The MSB b7 is sent first.

Table 4 Operating Mode

Mode	$R\overline{W}$ bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	1 to 4096	Similar to Current or Random Mode
Byte Write	'0'	1	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	8	START, Device Select, $R\overline{W}$ = '0'

Table 5 Endurance and Data Retention

Device	Endurance E/W Cycles	Data Retention Years
ST14/15E32F	1,000,000	10

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 5 AC Testing Input & Output Waveforms

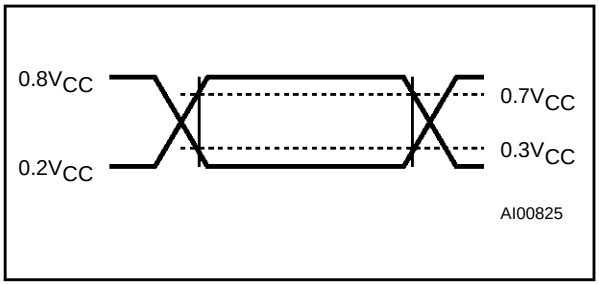
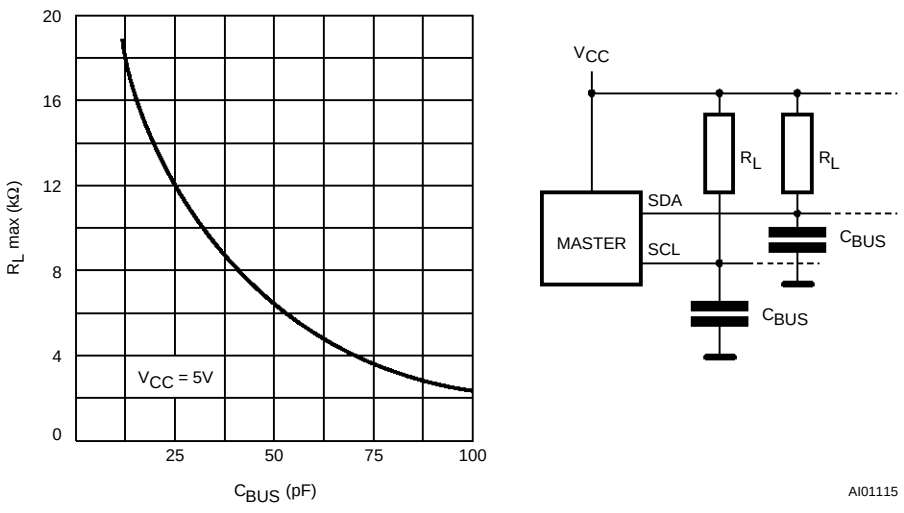


Figure 6 Maximum R_L Value versus Bus Capitance (C_{BUS}) for an I^2C Bus



1 SIGNALS DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 6).

Serial Data (SDA)

The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 6).

Write Control ($\overline{WC}$)

The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH} or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL}.

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the Application Note AN404 for more detailed information about Write Control feature.

Table 6 Input Parameters
(TA = 25°C, f=400KHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Table 7 DC Characteristics
(T_A = 0 to 70 °C ; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC,}$ SDA in H_i-Z		± 2	µA
I_{CC}	Supply Current ST14E32F	f_c = 400kHz (Rise/Fall time <30ns)		2	mA
	Supply Current ST15E32F			1	mA
I_{CC1}	Supply Currrent (Standby) ST14E32F	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5V, f_C= 400 kHz		300	µA
I_{CC2}	Supply Currrent (Standby) ST15E32F	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.7V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.7V, f_C= 400 kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input HighVoltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PRE, MODE)		- 0.3	0.5	V
V_{IH}	Input High Voltage (PRE, MODE)		V_{CC} - 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage ST14E32F	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage ST15E32F	I_{OL} = 2.1mA, V_{CC} = 2.7V		0.4	V

Table 8 AC Characteristics

(T_A = 0 to 70 °C ; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2}	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W (2)	t_{WR}	Write Time		10	ms

NOTES :

1) For a reSTART condition, or following a write cycle.

2) In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms

2 DEVICE OPERATION

I2C Bus Background

The ST14/15E32F support the extended addressing I2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST14/15E32F are always slave devices in all communications.

Start Condition

START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST14/15E32F continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST14/15E32F and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input

During data input the ST14/15E32F sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection

To start communication between the bus master and the slave ST14/15E32F, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ (RW = 1) or WRITE (RW = 0) operation. There are two modes both for read and write. These are summarised and described hereafter (see Table 4).

A communication between the master and the slave is ended with a STOP condition.

Memory Addressing

A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b11,b10,b9,b8 of the Most Significant Byte select one block among 16 blocks (one block is 256 bytes).

Table 9 Most Significant Byte

X = Do not care

X	X	X	X	b11	b10	b9	b8

Table 10 Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST14/15E32F acknowledge this and wait for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 16 blocks of 256 bytes each. Writing in the ST14/15E32F may be inhibited if input pin WC is taken high.

For the ST14/15E32F versions, any write command with WC = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes (see Figure 10).

Figure 7 AC Waveforms

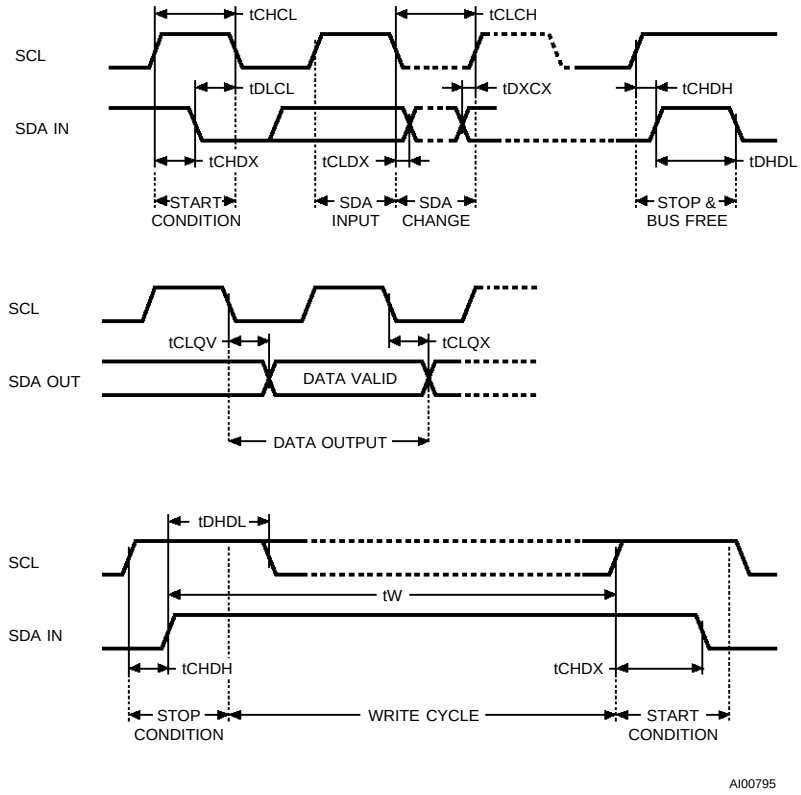
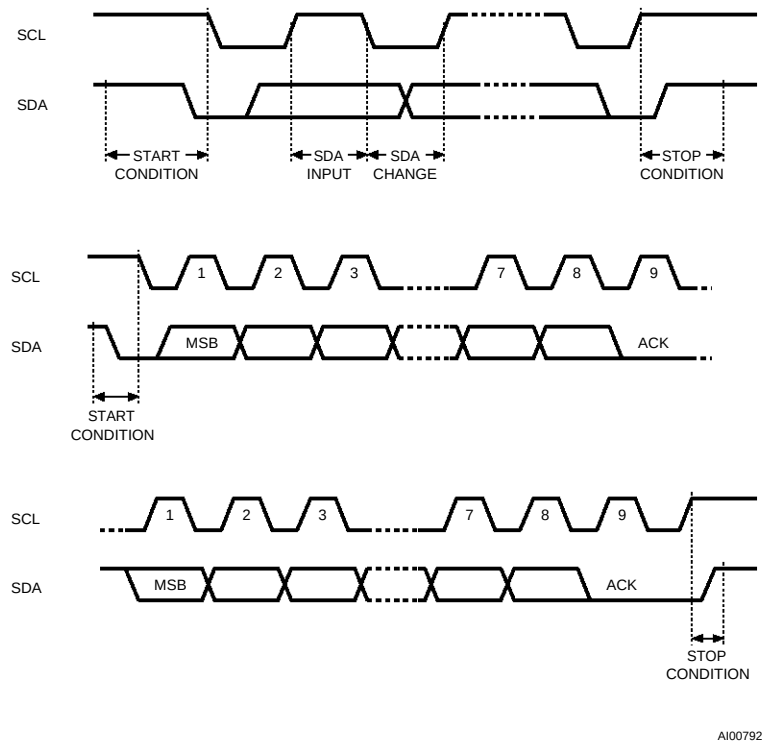


Figure 8 I^2C Bus Protocol



Byte Write

In the Byte Write mode the master sends one data byte, which is acknowledged by the ST14/15E32F. The master then terminates the transfer by generating a STOP condition.

Page Write

The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b11 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the ST14/15E32F.

After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST14/15E32F will not respond to any request.

Minimizing System Delay by Polling On ACK

During the internal Write cycle, the ST14/15E32F disables themselves from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

Initial condition: a Write is in progress

(see Figure 9).

- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST14/15E32F are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST14/15E32F have terminated the internal writing, it will issue an ACK. The ST14/15E32F are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read

The ST14/15E32F have an internal 12 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the RW bit set to '1'. The ST14/15E32F acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read

A dummy write is performed to load the address into the address counter (see Figure 11 and Figure 12). This is followed by another START condition from the master and the byte address repeated with the RW bit set to '1'. The ST14/15E32F acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST14/15E32F continue to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode

In all read modes the ST14/15E32F wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST14/15E32F terminates the data transfer and switch to a standby state.

Figure 9 Write Cycle Polling using ACK

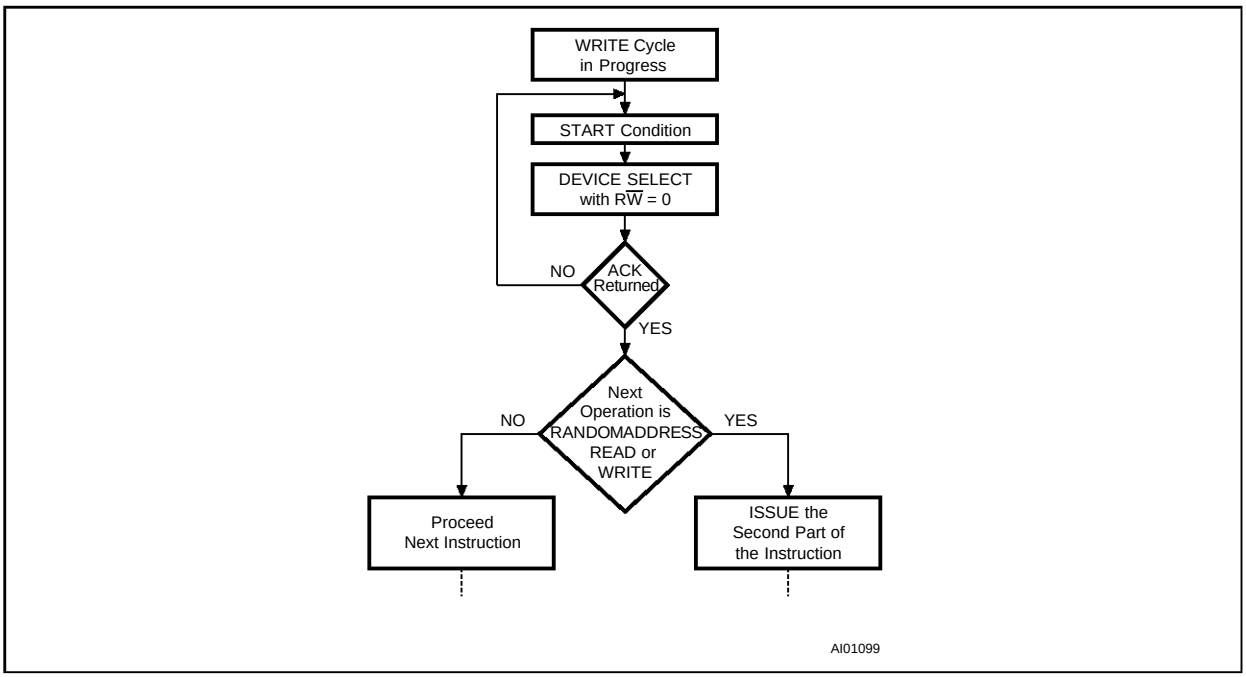


Figure 10 Write Modes Sequence

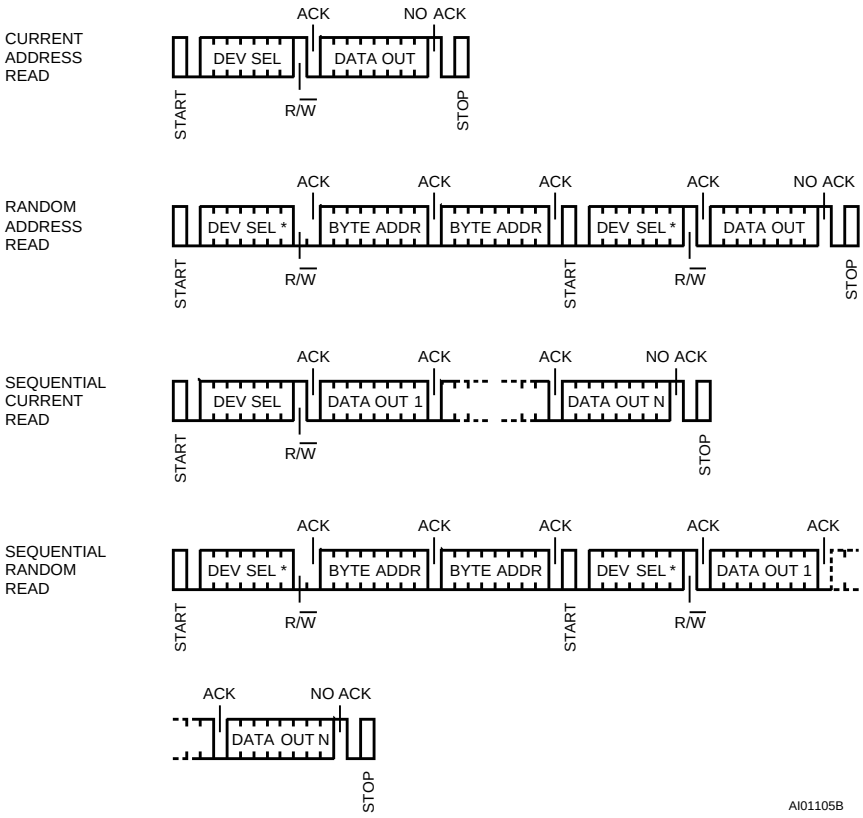


Figure 11 Read Mode Sequence with Write Control = 0

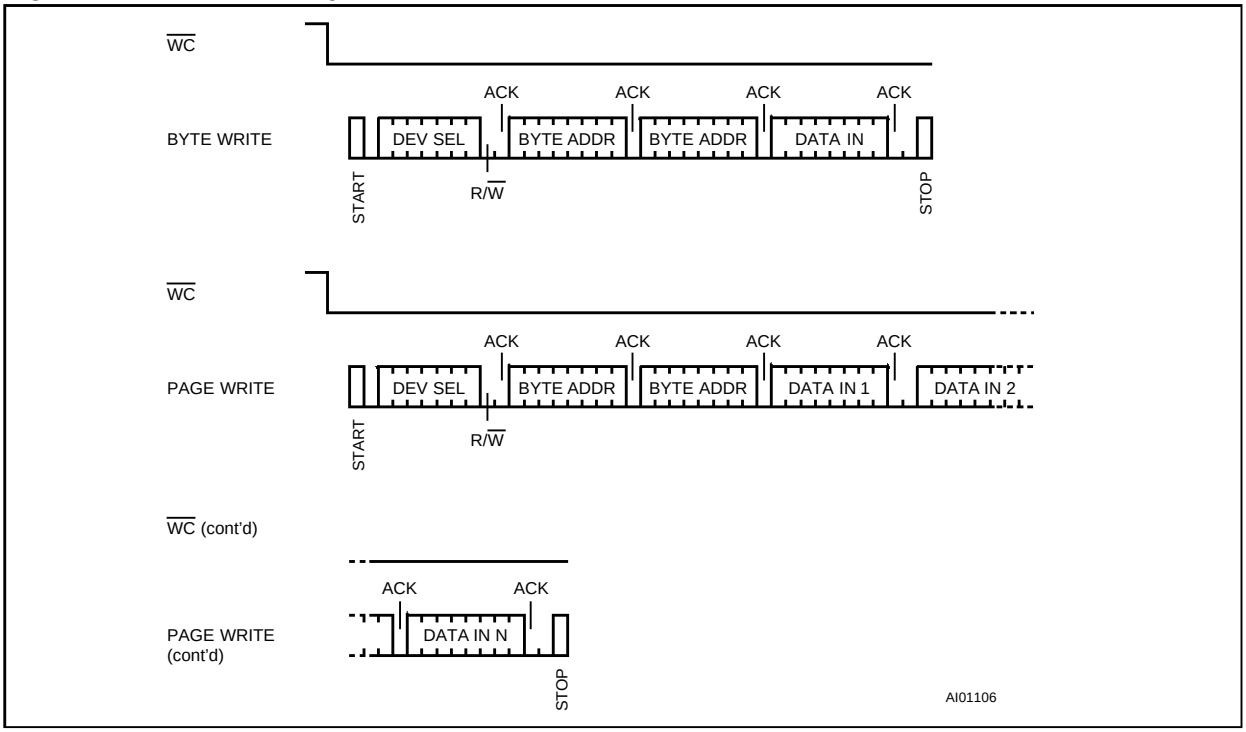
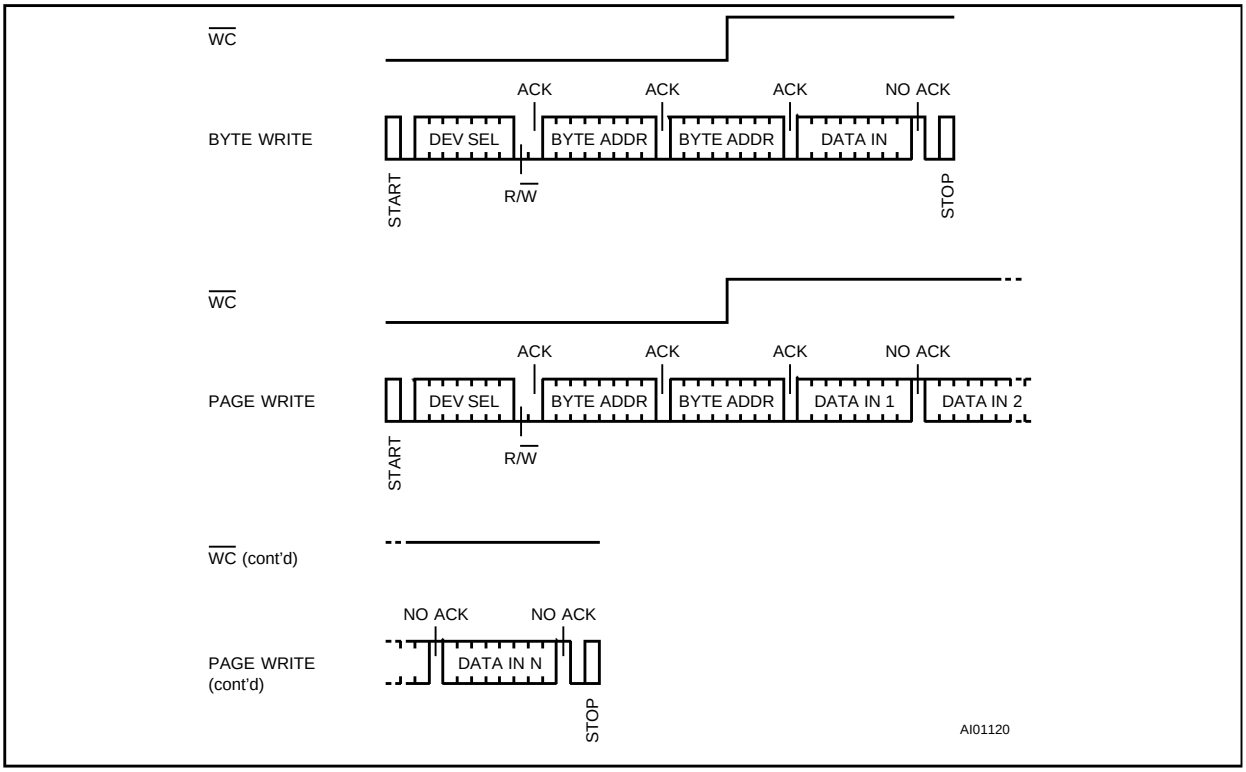


Figure 12 Read Mode Sequence with Write Control = 1



3 ORDERING INFORMATION

Table 11 Sales Types Available

SAWN WAFER	UNSAWN WAFER	MODULES
ST14E32FS21 ST15E32FS21	ST14E32FW2 ST15E32FW2	ST14E32FD10 ST15E32FD10
ST14E32FS22 ST15E32FS22	ST14E32FW4 ST15E32FW4	
ST14E32FS23 ST15E32FS23		
ST14E32FS24 ST15E32FS24		
ST14E32FS41 ST15E32FS41		
ST14E32FS42 ST15E32FS42		
ST14E32FS43 ST15E32FS43		
ST14E32FS44 ST15E32FS44		

Note :

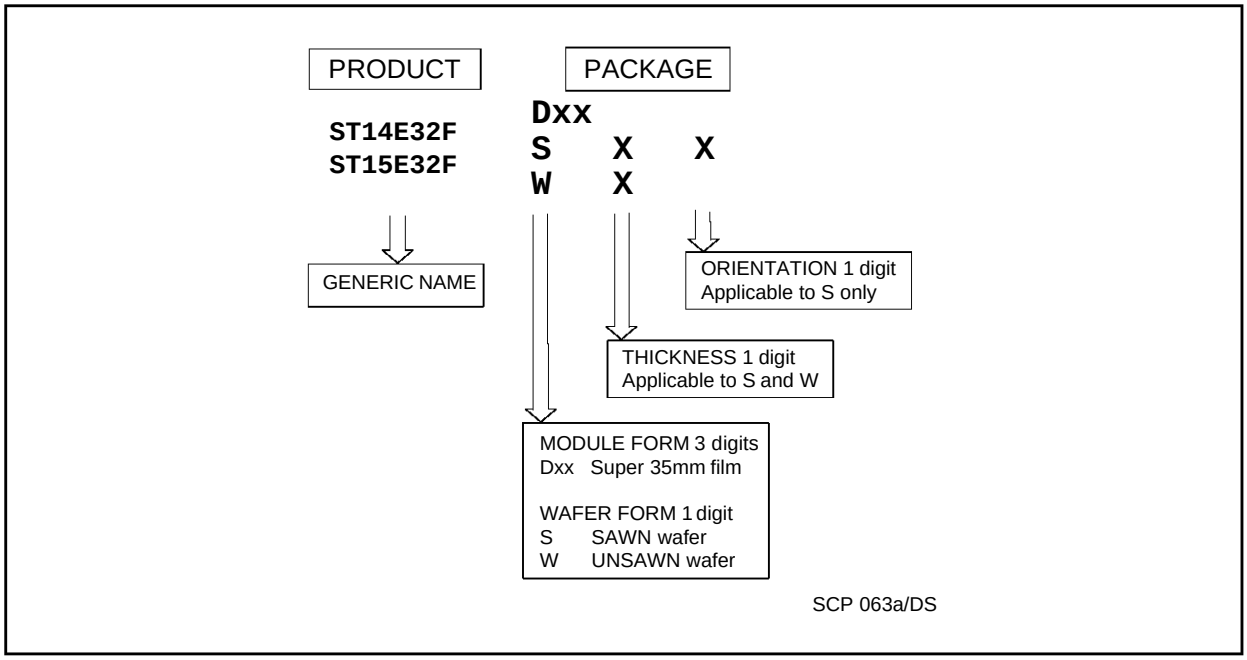
– Parts are shipped with the memory content set at all “1’s” (FFh).

– For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

Table 12 Wafer Thickness

THICKNESS	UNSAWN	SAWN
275µm ± 25µm	W2	S2
180µm ± 15µm	W4	S4

Figure 13 Sales Types Architecture



3.1 Sawing Orientation

Sawn wafers are scribed and mounted on adhesive tape into a frame. The orientation of the die with respect to the plastic frame notches has to be specified by the Customer.

The orientation is defined by the position of the GND pad of the die versus the notches of the frame, active area of product visible.

Caution : Wafers mounted on adhesive tape must be used within a limited period after the mounting date :

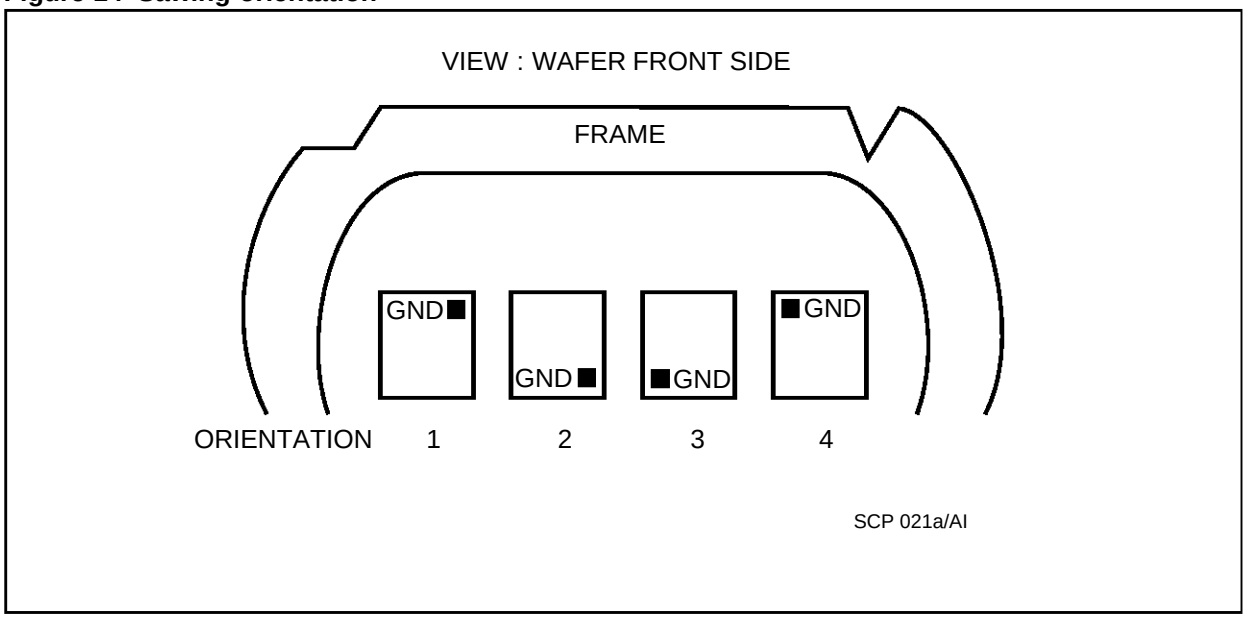
– 2 months,
if wafers stored at 25°C, 55% Relative Humidity

– 6 months,
if wafers stored at 4°C, 55% Relative Humidity

Table 13 Sawing codes

ORIENTATION	CODE
GND top right	1
GND bottom right	2
GND bottom left	3
GND top left	4

Figure 14 Sawing orientation



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